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QUESTRON CORPORATION
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ELECTRONIC SUBSYSTEM ANALYSIS
(ESA)

FINAL TECHNICAL REPORT

CDRL ITEM A002

February 1977

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This technical report has been reviewed and is approved for distribution.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The Electronic Subsystem Analysis Program was a twenty-four month effort funded by U.S. Air Force Space & Missile Systems Organization (SAMSOTR), Reentry Systems and Minuteman deputates. The program required that studies analysis and trade-offs of systems and subsystems technology for reentry systems and advanced guidance systems be conducted. These studies and analysis required in-depth investigations into such areas as: system and subsystem integration, semiconductor and integrated circuit technologies, computer architecture and configurations, nuclear harding processes and techniques, and terminal guidance sensor systems. This report documents the efforts of the Quesstron Corporation during the period of performance relative to the technology tasks performed and the results and recommendations tendered.		

TABLE OF CONTENTS

	Page No.
1.0 Introduction	4
1.1 General Background	4
2.0 Overview	5
3.0 Majority Carrier Devices	7
3.1 Logic Implementation	12
3.2 Memory Implementation	16
3.3 Charge Coupled Devices	20
4.0 Minority Carrier Devices	21
4.1 Radiation Effects	23
4.2 Logic Implementation	25
4.3 Memory Implementation	30

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List of Figures

Title

MOS Transistor Structure	Figure 3.1
CMOS Transistor Structure	Figure 3.2
General Processing Unit	Figure 3.3
MNOS Transistor Structure	Figure 3.4
Monolithic Integrated Circuit Transistor Structure	Figure 4.1
Standard Materials Isolation Process	Figure 4.2
Bipolar Logic Structures	Figure 4.3
Technology Comparison	Figure 4.4
Sample Parts List	Figure 4.5

List of Acronyms

ESA	Electronic Subsystem Analysis
SAMSO	Space and Missile Systems Organization
RS	Reentry Systems
ABRES	Advanced Ballistic Reentry Systems
RADC	Rome Air Development Center
TAP	Technology Applications Program
MOS	Metal-Oxide-Semiconductor
SOS	Silicon-on-Sapphire
CMOS	Complementary Metal-Oxide-Semiconductor
MNOS	Metal-Nitride-Oxide-Silicon
FET	Field Effect Transistor
NDRO	Non-Destructive-Read-out (Memory)
RAM	Random Access Memory
ROM	Read Only Memory
LSI	Large Scale Integration
GPU	General Processing Unit
ULA	Universal Logic Array
CCD	Charge Coupled Device
TTL	Transistor-Transistor Logic

ELECTRONIC SUBSYSTEM ANALYSIS

1.0 INTRODUCTION

→ The Electronic Subsystem Analysis (ESA) program was a twenty-four month effort from March 1975 through March 1977. The principal activities were conducted for the Space and Missile Systems Organization, Deputy for Re-entry Systems (SAMSO/RS) with supplemental activities conducted for SAMSO, Deputy for Minuteman, the MNNG office. Studies and analyses performed during the ESA program included:

- Analysis of emerging integrated circuit technologies
- Analysis of semiconductor technologies relative to booster and terminal guidance systems

1.1 General Background

→ The Electronic Subsystem Analysis program is part of the Advance Ballistic Re-entry System (ABRES) re-entry guidance and electronics activities for the establishment of the technologies required to build advanced re-entry guidance systems with the required performance, reliability, and radiation hardness while minimizing size, weight, power and volume. This program is designed to appraise critical technologies, subsystems, and provide design alternatives to assist ABRES personnel in defining performance criteria for components and subsystems and planning future activities. This effort was a follow-on to the Technology Applications Program IV (TAP IV) (F04071-73-C-0294). In November, 1976 the ESA Program was supplemented with the SAMSO/YAD Fault Tolerant Spaceborne Computer program to provide engineering studies and analysis.

2.0 OVERVIEW

One of the most important, and yet often overlooked topics for any missile or satellite SPO at SAMSO, is the real-world state of the art in military integrated circuit technology. These insignificantly small devices (usually less than 1/4 inch square) have caused more system level grief than nearly any other system component-usually by their absence. A recent example is the medium scale integrated circuits developed by Lockheed for the Trident auto-pilot computer. Tens of millions of dollars and over three years have been expended in the development of these devices, with adequate results yet to be obtained. The underlying problem with this effort was an unrealistic technical assessment by Lockheed of the real world state-of-the-art in relation to system-imposed operational requirements. One of Questron's prime responsibilities is to provide SAMSO sufficient information to avoid such a quagmire of specmanship vs technology limitations which often leads to schedule slippages and excessive costs.

The real world of integrated circuits must be evaluated from the anticipated users point of view. Although a common base with commercial processing is always desirable, radiation and reliability criteria usually (but not always) dictate important modifications to the standard processes. SPO requirements include the following topics:

- *PERFORMANCE*
 - Speed
 - Size, Weight, Power
- *ENVIRONMENT*
 - Reliability
 - Radiation
- *PRODUCTION*
 - Short (1 - 2 years)
 - Medium (2 - 5 years)
 - Long (>5 years)
- *COST*
 - Initial
 - Life Cycle

The following technology review is divided into two major sections. The first addresses a review of majority carrier devices such as CMOS logic and MNOS memories. The second section is concerned with minority carrier devices such as bipolar transistors, transistor-transistor logic and integrated injection logic. Included in each section are discussions of basic device physics, new technological advancements, radiation effects and reliability considerations. For brevity, it has been necessary to forgo the pleasure of detailed mathematical derivations and extensive analysis. Every effort has been made to limit the scope of this review to those issues which directly address in a qualitative manner the criteria listed above.

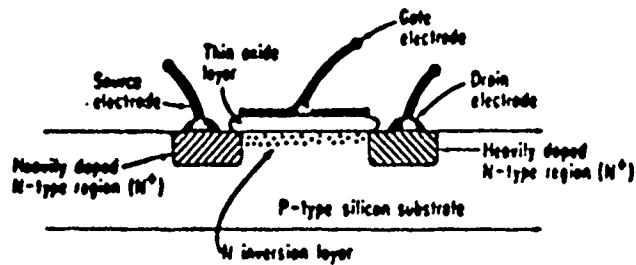
3.0 MAJORITY CARRIER DEVICES

The operation of majority carrier devices can best be described by referral to figure 3.1(a) which depicts a N-channel metal-oxide-semiconductor (NMOS) transistor fabricated on bulk silicon. The following discussion is applicable to an P-channel device if the appropriate reversals in bias polarities and dopants are made. As seen in figure 3.1(a), an NMOS transistor is fabricated on a P⁻ wafer of silicon by heavily doping two closely spaced regions with an N⁺ dopant (these areas are called the source and drain). A metal plate is positioned between the two N⁺ regions in close proximity to the silicon surface but insulated by a thin SiO₂ layer (800Å to 1200Å thick). With no voltage applied to this gate electrode, the two N⁺ regions can support a large reverse bias due to the two back-to-back P/N⁺ junctions. However if a small positive bias is applied to the gate, the surface of the silicon begins to accumulate electrons (figure 3.1(b) and 3.1(c)). With sufficient potential, the entire surface between the source and drain will become N⁺ in nature thus effectively shorting the two N⁺ regions. Therefore the NMOS transistor has been turned on by a positive potential applied to the gate electrode.

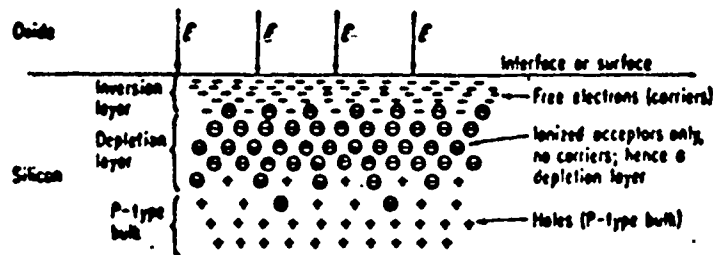
Recent improvements to the basic MOS device include the following:

- The use of silicon rather than aluminum for the gate material,
- Ion implanted source and drain regions,
- Dielectrically isolated transistors.

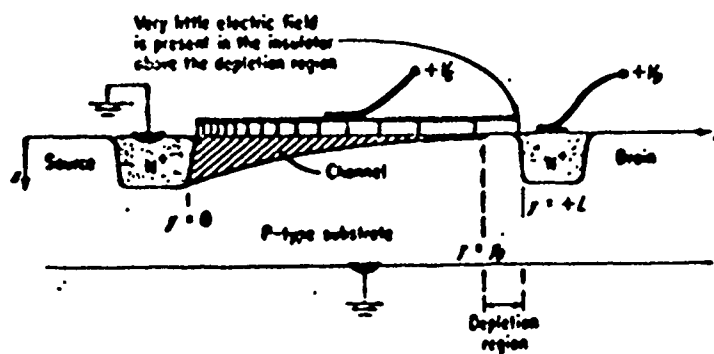
The use of a doped polysilicon gate enhances transistor performance through an increase in switching speed and also permits a more densely packed integrated circuit via the use of a second level of interconnect (polysilicon). Ion implantation is essentially a precisely controllable pre-deposition of the required dopants. It's use increases device yield and minimizes the required dopant drive-in time/temperature product. Experiments have shown this to be beneficial in reducing MOS radiation sensitivity.



MOS transistor structure.



Charge distribution near the silicon surface.



The shape of the channel at pinch-off.

MOS Transistor Structure

Figure 3.1

The fabrication of MOS devices in a thin ($\sim 1\mu$) epitaxial film grown on a sapphire substrate (depicted in Figure 3.2) is an important variation in MOS technology from both a military and commercial point of view. The use of sapphire greatly reduces the node capacitances and provides greater on-chip speed than is normally achievable with bulk MOS devices. In addition, certain aspects of radiation tolerance are greatly enhanced. The major drawbacks to the silicon-on-sapphire (SOS) technology include stringent process controls, reduced carrier mobilities due to poor quality epitaxial crystal structure and potential back-channel (Silicon-Sapphire) leakage problems (discussed below).

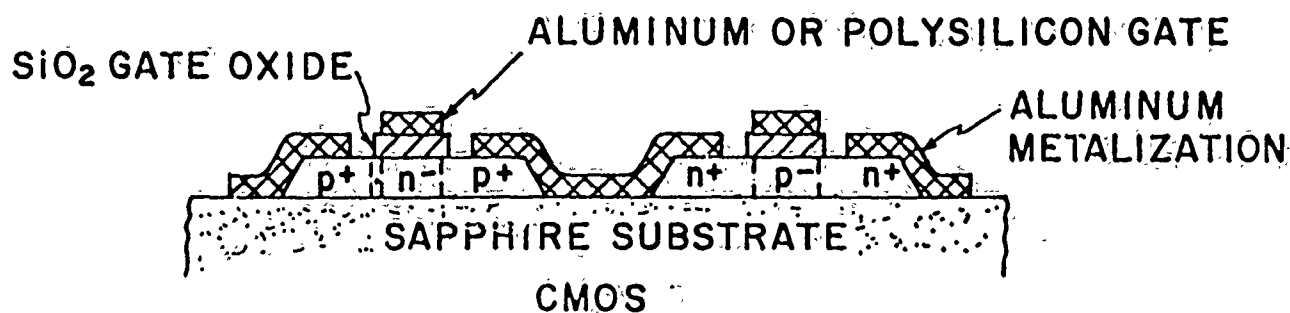
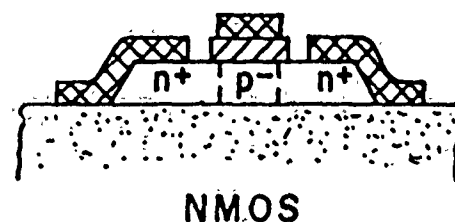
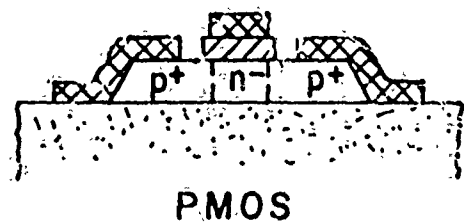
Radiation effects on MOS devices include the following:

- Total Dose
- Dose Rate
- Neutrons

Because MOS technology is based on majority carrier physics, neutron induced lattice defects do not cause appreciable degradation in performance. This is due to a lack of minority carriers for recombination processes in the channel region during device conduction.

Transient radiation effects are more pronounced in CMOS bulk devices than CMOS/SOS due to the larger current collection areas (P-N junctions). Logic upset levels for bulk CMOS range from 10^6 rad(si)/sec to mid 10^8 rad(si)/sec. SOS devices usually do not upset below mid 10^9 rad(si)/sec and have, through careful design, reached mid 10^{11} rad(si)/sec upset levels. Another major drawback to bulk devices is the possibility of a four-layer latch-up action. This is totally eliminated by SOS (dielectric isolation).

Total dose effects are primarily concerned with charge build-up in the gate oxide and sapphire. Under radiation, electrons and holes are formed in the insulating materials. The nature of the trapping sites in the insulators is such that electrons freely escape but holes are trapped and create a space charge which decays with time after irradiation. In the gate oxide, this results in a shift of the gate potential required to turn the MOS device on or off. If this shift is too large, the device will cease to function. Charge trapped in the sapphire can invert the back channel silicon-sapphire interface and cause a moderate-to-large leakage current to flow. Recent



CMOS Transistor Structure

Figure 3.2

advances in metal gate MOS device technology (both bulk and SOS) have increased the radiation tolerance to over 10^6 rad(si). At present, silicon gate devices are only radiation hard to mid 10^5 rad(si) although considerable research is underway to improve this.

In addition to the trapped charge problems discussed above, there is currently a great deal of interest in the physical aspects of radiation-induced interface (IF) states at the SiO_2 -Si interface. These states cause threshold voltage shifts similar to that caused by trapped oxide charge and, in addition, reduce the majority carrier surface mobility. A recent (July 1976) radiation hardening conference included an interesting report by Harry Diamond Laboratories which proposed that IF states are created by the passage of radiation-induced holes past the SiO_2 -Si interface rather than radiation itself.

Since its identification as a potential radiation effects problem several years ago, rapid annealing of the MOS threshold shift immediately after an exposure has received considerable attention. Investigative techniques are predominately based on freezing in the radiation-induced holes at 80°K and then slowly heating the sample while monitoring the thermally (and sometimes electrically) emitted charge. It is apparent that a qualitative understanding exists for the phenomenon, but a quantitative explanation must wait for more detailed information regarding the spacial and energetic distribution of the relevant hole traps.

Experimental studies of the time dependence of the radiation induced MOS threshold voltage shifts have shown that it is entirely possible to have a device which is insensitive to total dose (to 10^6 rad(si)) several hours after irradiation but which shows large (3 to 4 volt) shifts in threshold potential for 10ms to 100ms after an exposure.

Little meaningful reliability data exists as of yet for CMOS devices because no major system has fielded the technology. Numerous laboratory studies have been conducted for bulk CMOS and some data exists for CMOS/SOS technology. The chief problem areas appear to be the gate oxide stability and the input protection networks. This assumes the devices have passed a minimal burn-in screen test since the real problem in CMOS/SOS is device producibility. RADC has published limited reliability studies and is currently studying evaluation standards for CMOS (both bulk and SOS) technology.

A paper by IBM at the International Reliability Conference (April, 1976) discussed possible instabilities in N-channel FETs due to hot electron injection into the gate insulator from the drain junction. If a portion of these electrons are trapped, the threshold may shift and the source-drain breakdown voltage may decrease. Data were presented to verify the theoretical models and to establish a long-term reliability vulnerability. Questron feels that although the data were taken with unusual bias conditions (+12V gate, +5V drain, -3V body) and the source-drain functions were reversed to enhance the effect, the reliability community will probably require *substantial* verification of the stability of any N-channel device to be fielded in a system, especially one with a sandwich gate insulator. Questron agrees with this position, and studies of hot electron injection instabilities should be included in near term MX development programs.

Questron conducted a survey of the current status of availability and reliability of commercial CMOS RAMS for SAMSO/ABRES. Brief discussions with Harris Corporation indicated failure rates of approximately 0.04% per 1000 hours at 25°C. Intersil has conducted reliability studies on their silicon gate CMOS 1K RAM (IM-6508). A synopsis of these studies is given below. The 6508 (military version) is screened to visual class B. A stabilization bake of 150°C for 24 hours is performed along with a 10 cycle (-65°C to 150°C) temperature cycle test. Life test data were taken in 1974 and 1975 on approximately 668 devices for 863,000 device hours. This evaluation resulted in a failure rate of 0.038% per 1000 hours at 60% confidence at 55°C — somewhat better than the Harris failure rate estimate.

The Intel reliability data is more extensive with some 60×10^6 device hours at 55°C. Calculated failure rates of 0.015% to 0.04% per 1000 hours at 90% confidence level at 55°C were obtained depending on the details of the CMOS technology used (enhancement or depletion mode transistors for example).

3.1 Logic Implementation

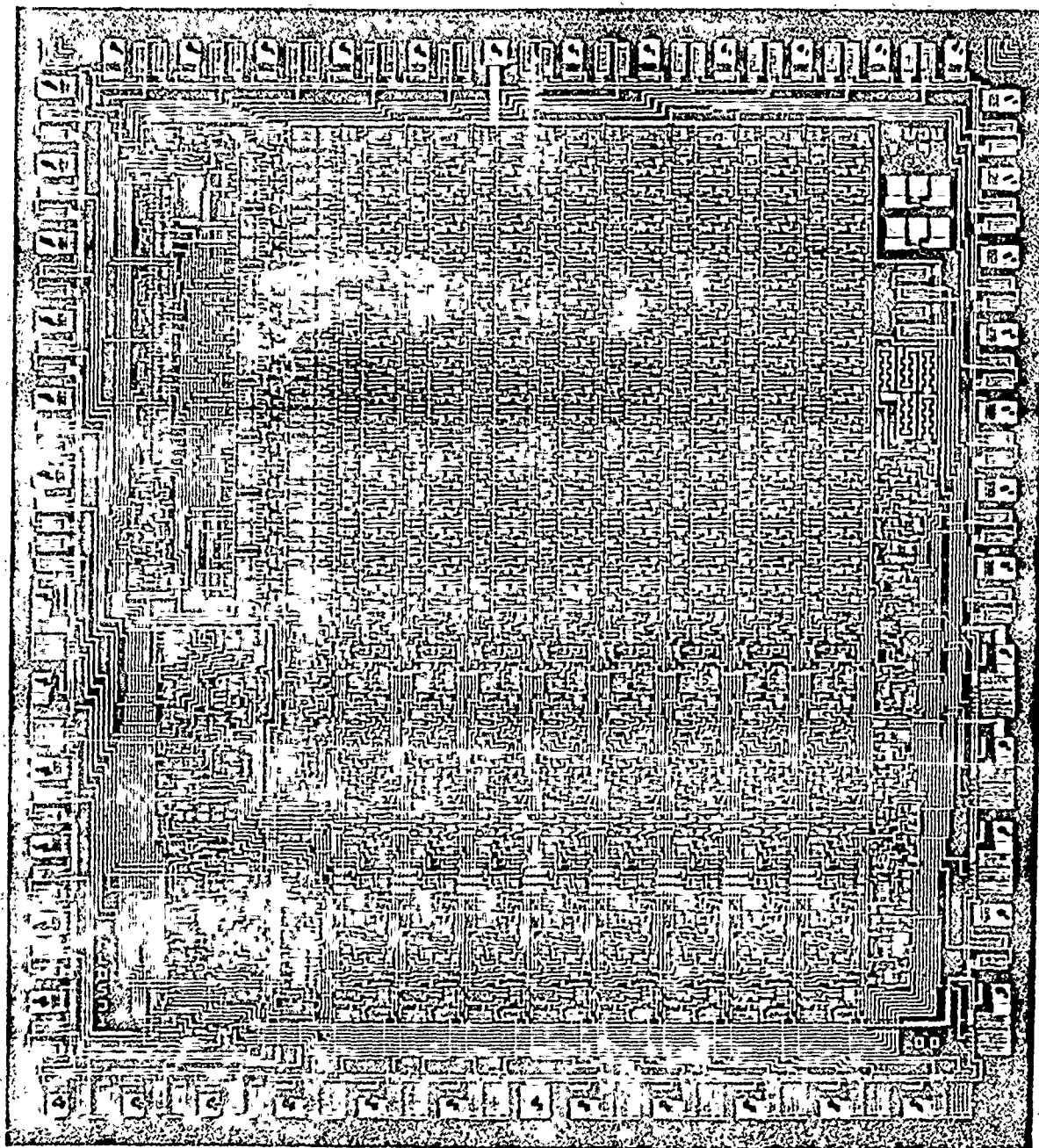
The conventional techniques for fabricating a logic gate (an inverter in this case) is shown in Figure 3.2. Although the figure depicts the SOS technology, a similar structure exists for bulk MOS technology. To form a complementary MOS (CMOS) inverter, a P-channel FET is connected in series with a N-channel FET. By connecting the open end of the P-channel

FET to +10 volts, the open end of the N-channel to ground and the gates of both devices together, the basic inverter structure is formed. If +10 volts appears on the common gates, the N-channel device conducts thus grounding the common P^+-N^+ node. The P-channel device provides isolation from the +10 volt supply. If 0 volts is applied to the gates, the N-channel device turns off while the P-channel device turns on and the output (P^+-N^+ node) rises to +10 volts. As can be seen, one of the major advantages of CMOS technology is that the only power it consumes is that required to charge and discharge the node capacitance. At low frequencies, CMOS power consumption is extremely low.

The speed with which the inverter can switch depends on the load capacity of this next pair of gates, the interconnect capacity and the ability of the PMOS and NMOS devices to supply charging and discharging currents. The ability to supply current increases markedly with decreasing channel length (distance between the two heavily doped regions) and increasing majority carrier mobility in the channel region (depends on crystal order in the epitaxial layer and the absence of interface states).

The highest achievable functionality (speed, packing density, etc.) of CMOS technology varies widely from manufacturer to manufacturer especially for SOS. In general, the highest performance can be obtained via custom designed Large Scale Integration (LSI) devices on sapphire. RCA is the current leader in this field and has recently fabricated the LSI general processing unit (GPU) shown in Figure 3.3. This device is the state-of-the-art in CMOS/SOS and could, if it were radiation hard, fulfill numerous SAMSO requirements. It should be noted that the original architecture for this device was completed by Questron and Tracor under ABRES sponsorship approximately two years ago.

The standard cell approach wherein a LSI circuit is fabricated from a limited number of pre-designed logic functions can achieve 50 to 80% of custom designed device capability. Universal logic arrays (ULA) consist of a large number (75 to 300) of elemental inverter nodes fixed on a chip and interconnected at the discretion of the designer. This approach entails an even greater performance penalty (30 to 60%) relative to custom designed circuits.



General Processing Unit

Figure 3.3

The problems associated with CMOS/SOS technology include the numerous (9 to 11) critical processing steps (low yield, lot-to-lot variations, "magic fingers syndrome"), the achievement of a radiation hard silicon gate process (total dose and rapid anneal of threshold voltages are the key areas) and declining commercial emphasis (Solid State Scientific has withdrawn from the market, leaving RCA as the sole commercial supplier of CMOS/SOS). If the current military efforts to develop this technology continue at the present level, Questron feels that the production schedule will fall between 2 to 4 years. That is, the technology should be mature enough to be seriously considered for production purposes. Today, a SPO can go to any of a number of contractors (Hughes, RCA and Rockwell for example) and, with sufficient funds, have fabricated 50 radiation hard samples of any given part. These would not be as complex as the custom designed GPU at RCA, but could certainly be a useful level of integration. The problem would arise when one begins to shift attention toward other system development problems and relax the IC effort.

The bulk CMOS technology offers much less production risk due to the large commercial market and the absence of silicon-sapphire interface. The chief disadvantages to CMOS/Bulk have been slow speed (relative to CMOS/SOS) and radiation sensitivity (low upset threshold and latch-up). Consequently, little LSI military emphasis for hardened systems has been placed in this technology in the past. Recently, Harris has developed a narrow-channel bulk CMOS process with outstanding speed performance. This technique has been proven in the commercial market, and Questron has tested several devices. Furthermore, Sandia has developed a gold doping process for bulk CMOS that eliminates latch-up and reduces photocurrents (i.e., increases the γ upset threshold). Currently, SAMSO/YAD and SAMSO/ABRES are funding an investigation designed to integrate these concepts with the objective of fabricating fast, radiation hard, bulk CMOS devices for military use. Results are expected by mid-1977.

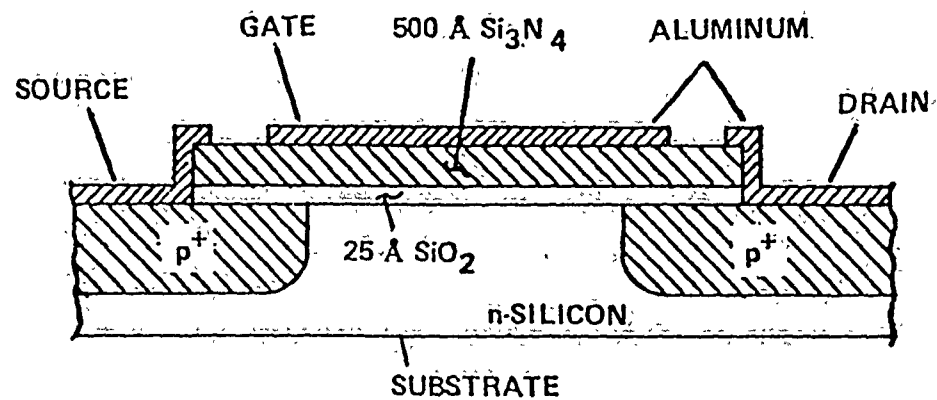
Questron has recently noted a new CMOS/Bulk process developed by RCA for their COSMAC II microprocessor called C²L (closed complementary logic). Initial speed performance is impressive and the technology should be investigated for possible use with gold doping.

3.2 Memory Implementation

The MOS field effect transistor (FET) lends itself well to the conventional static memory cell (flip-flop circuit) and several commercial Random Access Memories (RAM) are available (both on bulk and sapphire). However, in military applications where nonvolatility is often a requirement, the MOS technology affords an interesting possibility. Since the threshold voltage (the gate potential required to turn the FET on) depends on the charge trapped in the gate oxide, it is possible to construct a single transistor memory cell that is both non-volatile and is not affected by reading its state (NDRO). Figure 3.4 is a schematic of the operation of such a device fabricated on bulk silicon. The gate insulator consists of a sandwich of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) (metal-nitride-oxide-silicon = MNOS). The oxide is thin enough (20Å) so that when a modest potential is applied between the gate and the FET body (20 to 30 volts), charge tunnels into the insulator and becomes trapped near the interface between the SiO_2 and Si_3N_4 . This charge remains trapped until a reverse voltage is applied to erase the memory. The state of the memory is sensed by determining the threshold potential of the transistor.

The operation of the memory device itself is relatively independent of the substrate material (silicon or sapphire), but on sapphire, the decode circuitry is much faster resulting in a low memory access time relative to bulk devices.

The chief MNOS characterizing parameters are retention and endurance. A high write potential will inject more charge in a short period and provide longer retention but will also degrade the insulator properties after numerous write cycles. Thus MNOS devices wear out after extensive use. It has been found that the better the wearout properties, the worse the charge retention characteristics. In particular, several MNOS manufactures have found the product of retention (in seconds) and the endurance (write cycles) is a constant and is approximately 10^{16} . The physics of this phenomenon is not clearly understood.



MNOS Transistor Structure

Figure 3.4

Within the past two years, there has been an outstanding increase in commercial interest in non-volatile semiconductor memories. Applications have been found in citizen-band radios, television sets, and pocket calculators. These fields in themselves should provide an adequate base for long-term commercial interest. In addition, National Cash Register has utilized MNOS memories in point-of-sale equipment for several years. A recent MNOS workshop (August 1976) reflected this intense interest with over one hundred attendees from many of the largest commercial concerns (IBM, National, Fairchild, NCR, etc.) and many countries (Japan was well represented).

The conference was organized around five key topics:

- Status of theoretical analysis.
- Processing parameters.
- Experimental analysis techniques.
- Reliability and radiation effects.
- Integrated circuit design and applications.

Although MNOS was the most popular memory element, other related technologies were discussed (FAMOS, avalanche injection, and Al_2O_3/SiO_2 gate structures were the most prominent). During the course of the conference, it became clear that for MNOS technology, device fabrication has progressed further than the knowledge of the physics of the material and a great deal of research is needed to understand quantitatively how MNOS devices function. This is even more crucial for MNOS than CMOS devices due to the necessity of accelerated test techniques for endurance and retention and due to the critical nature of the thin sandwich insulator construction necessary for MNOS. As of August, 1976, only the SAMSO ACT I program and the Weapons Laboratory were sponsoring MNOS/SOS developments and only ACT I has been attempting to fabricate a fast MNOS RAM on sapphire. Aside from Westinghouse, there was general pessimism regarding the success of the MNOS RAM with the current state-of-the-art. Westinghouse's differential write technique is unique and, at the present, is the only way a useful write cycle RAM can be constructed from MNOS technology.

At least six MNOS theories were discussed and compared. Each applies to some specific test condition or environment and can adequately represent only *that* situation. No attempt was made to generate a "universal MNOS" theory — due primarily to gross differences in processing details which result in variations in electron/hole trap distributions, band structures, etc.

Key issues discussed during the theoretical portion of the conference included the following:

- Extrapolation of retention data is not warranted by present knowledge of the physics of charge storage,
- The initial threshold window has little effect on long term retention (IBM philosophy),
- Most theories reduce to a common set of predictions in the limit of very long or very short write pulses.

There was some interest (primarily Bell Labs) in the use of Al_2O_3 in place of the Si_3N_4 insulator although little information was presented to directly compare the two technologies. Several papers dealt with the identification and elimination of contamination during the SiO_2 , Si_3N_4 and/or Al_2O_3 deposition.

One of the most startling papers of the conference was delivered by RCA and concerned the true nature of the thin (10 to 50Å) SiO_2 layer. It was proposed that this layer was not SiO_2 at all, but rather a diffuse silicon and nitrogen rich layer whose band structure and insulating properties remain essentially unknown.

Reliability data for bulk MNOS fielded by NCR in point-of-sale terminals was quoted by Sperry to be approximately .008% per 1000 hours at 60% confidence level. This is the only published reliability data known to Questron for MNOS devices. Since potential problems related to sapphire and the fast write mode of operation currently pursued by ACT-I are not included, it is probable that this figure can be used as an optimistic reliability goal.

Finally, there were numerous device papers wherein operational characteristics for several military contractor products were discussed, modeled and compared to competing designs. One rather interesting concept involves a current Westinghouse contract with the Air Force to develop a fast write volatile RAM with an intermixed MNOS EAROM. On command, total data transfer to non-volatile storage is executed in one write cycle for the entire memory. This technique could be useful in a true hardware circumvention and recovery system.

3.3 Charge Coupled Devices

A charged coupled device (CCD) consists of an array of narrow conducting plates positioned in close proximity (800Å to 1200Å) to a lightly doped wafer of silicon. The plates are usually grouped in units of three and the units are repeated several hundred times across the silicon chip. If three related potentials are applied to each unit ($V_1 = V_3 > V_2$) and charge is deposited in the potential well formed by V_2 , it will remain trapped beneath this plate until the potential bias are changed. It is possible to move this trapped charge packet along the line of plates by judiciously varying the applied potentials. Thus the CCD is related to the fact that they can store and transfer charge signals that have been introduced either electrically or optically.

CCDs have found applications in area-image sensors, serial memories and transversal filters. Analog filter systems based on CCDs are smaller and cheaper than the conventional methods which employ analog-to-digital conversion, digital manipulation with a computer and digital-to-analog reconversion.

Currently, CCD area-image sensors are being developed by Fairchild, RCA, TI, Bell Labs and GE. High density memories are manufactured by Fairchild, Intel and Bell Northern-Research. Transversal filters are being developed by General Electric and TI.

The radiation-induced upset level for CCDs is extremely low. One to ten rad(si) will fill the potential wells with charge and render the device inoperative until the potential wells can be electrically emptied. The total dose radiation sensitivity (permanent effects) is similar to the discussion for conventional MOS devices. Neutron effects have not yet been extensively addressed.

4.0 MINORITY CARRIER DEVICES

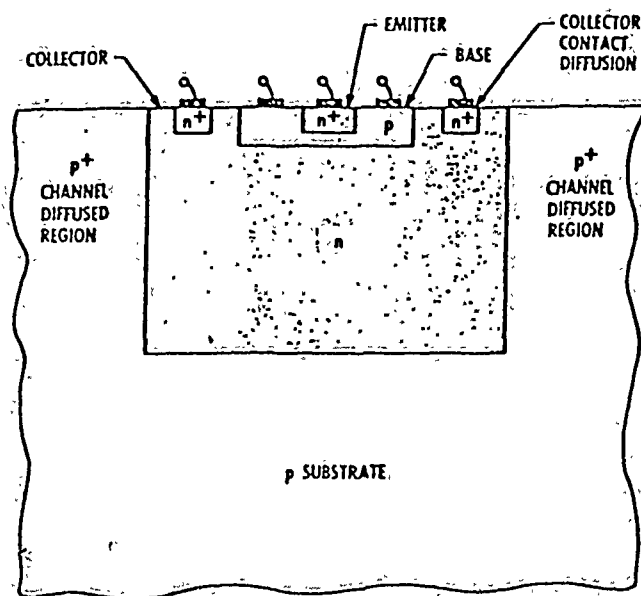
For the purposes of this report, minority carrier devices will imply integrated circuits constructed using bipolar transistors (either NPN or PNP type). Figure 4.1 is a schematic of a NPN bipolar transistor fabricated in bulk silicon. The device consists of an emitter, a base and a collector. Under appropriate biasing conditions, electrons leave the emitter, travel through the base (since the base is P-type material, the electrons are minority carriers in this region) and are collected by the large N-type region (collector).

The ratio of the current injected into the base to the current flowing from the emitter to the collector is the transistor gain. High gain devices usually have narrow base widths to minimize losses due to minority carrier recombination in the base region.

One of the limiting factors in the switching speed of a bipolar transistor is the time required to establish and then remove the charge stored in the depletion volume between the base and the collector. Switching speeds of 10 to 20ns are common unless specific steps are taken to reduce this stored charge. One technique consists of lightly doping the collector region with gold atoms. This effectively reduces the depletion volume and increases the speed of the transistor. Care must be taken not to introduce gold into the base region as this greatly increases recombination losses.

Another common technique consists of adding a special diode between the base and the collector. This device is called Schottky diode and, depending on its construction, conducts at 0.2 to 0.4 volts instead of the normal 0.75 volts for P-N junctions. This voltage clamping action between the base and collector prevents the formation of a large depletion volume and greatly speeds the switching action. Both techniques are currently in production for major systems and are discussed below:

Recently ion implantation of base and emitter dopants has been actively investigated as an improved processing technique.



Monolithic Integrated Circuit Transistor Structure

Figure 4.1

4.1 Radiation Effects

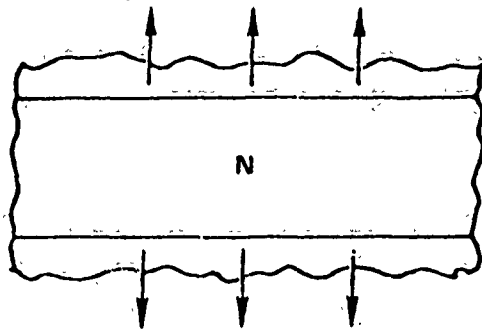
Since most bipolar devices do not depend on charge transport near this silicon surface, total dose effects are minimal. Occasionally charge trapped in the field oxide near a P-N isolation junction will cause leakage and possible field inversion. This problem is fairly well understood in the industry and with minimal care, devices can be constructed that will operate to 10^6 rad(si).

On the other hand, bipolar devices are very sensitive to neutron displacement damage in the base region and in the lightly doped collector region. Silicon damage in the base results in a severe loss in transistor gain while collector damage increases the collector-to-base saturation voltage (reduced noise margin). Unhardened bipolar devices often cease functioning below 10^{13} neutron/cm² (1MEV equivalent) while current hardened devices (narrow bases and specially doped collectors) operate up to mid 10^{14} neutron/cm².

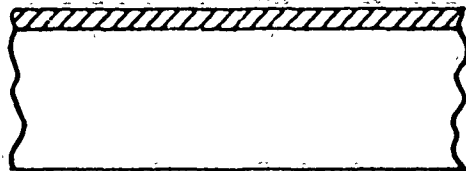
Transient radiation effects are similar to those discussed in bulk CMOS devices. For bulk devices, radiation induced photo-currents can cause logic upset between 10^6 and 10^7 rad(si)/sec and the potential for four-layer latch-up action exists.

To alleviate this sensitivity and the latch-up problems, the military has financed the development of dielectrically isolated (DI) bipolar devices. This technology is based on fabricating each transistor in its own isolated tub of epitaxially grown silicon as shown in Figure 4.2. Unfortunately, this isolation does not come free. Reduced packing density preclude fabrication of true LSI devices, and the cost for medium scale integration (MSI) chips is on the order of \$100 each. One of the biggest problems with DI technology is low yield due to the fabrication technique used in forming the dielectrically isolated tubs of silicon. Several manufacturers are working on new dielectric isolation processes but to Questron's knowledge, only TI (a sense amplifier program with AFML) is Air Force funded.

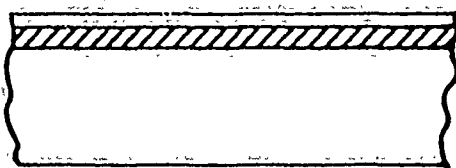
Step 1. Surface Preparation



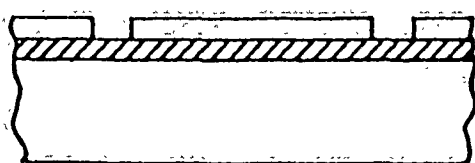
Step 2. N^+ Deposition



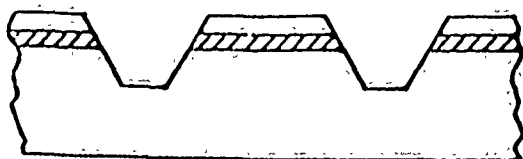
Step 3. Masking Oxide



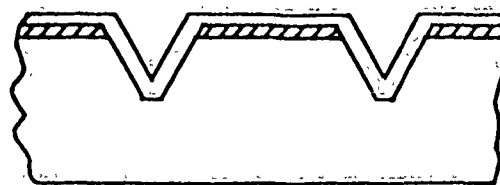
Step 4. Isolation Pattern



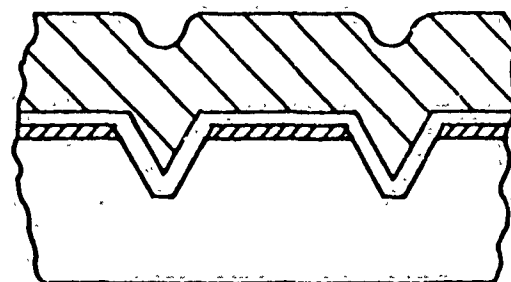
Step 5. Moat Etch



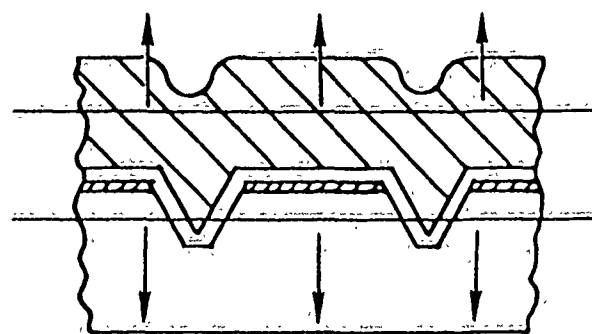
Step 6. Dielectric Oxide



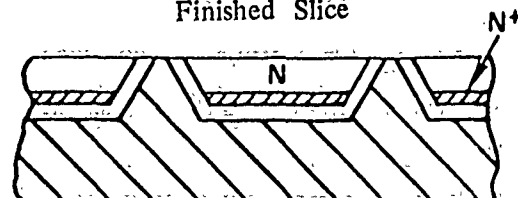
Step 7. Poly Deposition



Step 8. Backlap and Polish



Finished Slice



Standard Materials Isolation Process

Figure 4.2

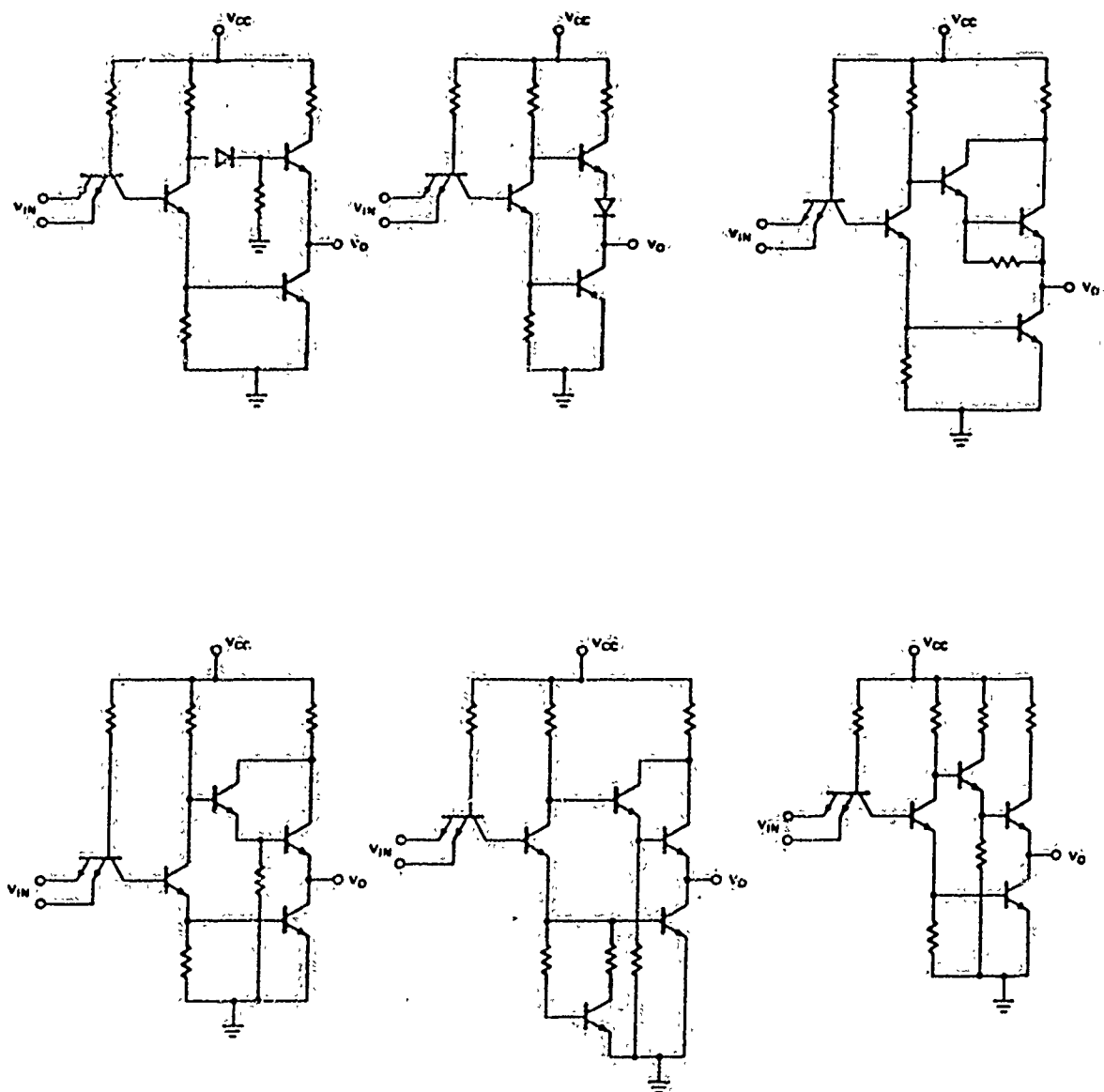
At this point, a few brief comments regarding linear circuits are in order. A heavily utilized part is the operational amplifier. There are numerous development programs at RCA, Harris, TI, and Motorola designed to fabricate radiation hard, fast operational amplifiers. At present, the most promising devices are the Harris operational amplifiers developed for Lockheed C-4 and for Northrop (different devices), and an RCA operational amplifier developed for the MK500 program at GE. Initial data at GE show excellent radiation hardness. Data on Harris devices is currently being taken by both customers.

At present, there is no source for radiation hard voltage controlled oscillators, video amplifiers, or line receivers—parts needed for analog signal processing. MX has identified a need for these parts and has initiated a development program at RCA and Motorola.

The four channel AC-coupled sense amplifier under development at TI by the Air Force Materials Laboratory is based on a new DI process wherein the epi is grown in the insulating boat to the desired thickness rather than ground down from a thicker epi layer. This process should permit the fabrication of very shallow (and radiation hard) transistors. The current TI schedule called for test bars by December 1976, and the first sense amplifier in the first quarter 1977. Questron is currently evaluating the most sensible procedure for SAMSO to assure the existence of a MX usable sense amplifier by mid-1978.

4.2 Logic Implementation

Currently, dielectric isolated transistor-transistor logic (T^2L) is the most popular bipolar circuit implementation for radiation hard system usage. Figure 4.3 represents typical realization of T^2L gates. The common elements are multiple emitter inputs and "totem pole" outputs. The Navy Trident program is presently using two forms of T^2L devices. The auto-pilot computer (Lockheed developed) is designed around the LMSC C-4 devices described in Figures 4.4 and 4.5. The Trident guidance computer has adopted the MSIA family of parts also described in Figures 4.4 and 4.5. The advanced Minuteman Missile-X (M-X) program has baselined low power Schottky T^2L devices similar to the LMSC C-4 technology. The primary changes involve the replacement of the gold beam lead bonding technique with conventional aluminum bonding pads.



Bipolar Logic Structures

Figure 4.3

Extensive reliability and radiation testing of the LMSC C-4 devices is currently underway at Lockheed as a part of a qualification program. Due to persisting difficulties in producing the LMSC C-4 parts, Lockheed has had to delay the completion of its qualification program several times. The Minuteman SPO has initiated an Air Force study of the modified LMSC C-4 devices (AIRS Parts) which will include producibility, device cost, radiation vulnerability and reliability.

The MSIA devices have completed a thorough reliability and radiation vulnerability program. The devices are currently in system use in the TRIDENT Guidance Computer.

Recently, a new logic implementation of bipolar technology has been introduced in the commercial and military markets. Because of the particular nature of the inverter geometry, it has been designated integrated injection logic (I^2L).

The primary disadvantage of I^2L (integrated injection logic) is its newness. At first, devices were relatively slow (20 to 30 ns/gate) and fairly neutron sensitive ($\sim 1 \cdot 10^{13}$ n/cm²). Its advantages include good packing density, few processing steps, and the ability to include digital and linear devices on a single chip. In 1975 Questron advised SAMSO that the super active commercial market should be closely watched by the military as speed will probably increase and if smaller transistors are implemented, radiation hardness may increase.

In response to this recommendation, funds from both M-X and DNA were directed to NWSC (Crane Ind.) to aid in assessment of the possible military uses of I^2L technology. NWSC has finished this study, and a final report has been reviewed by Questron personnel. Below are a few conclusions drawn from the contents of the report.

With the possible exception of transient upset levels, commercial I^2L LSI devices could probably meet many Air Force system needs. In order to meet the more severe military hardening requirements, several experimental I^2L configurations exist and a development program designed to evaluate the LSI potential of these geometries should be instituted. A few of these experimental structures have demonstrated sufficient neutron and total dose tolerance to be of use to reentry systems.

TECHNOLOGY COMPARISON

LMSC C-4	CSDL MSIA
• Low Power Schottky T ² L	• Standard T ² L
• Dielectric Isolation	• Dielectric Isolation
• Diffused Resistors	• NiCr Thin Film Resistors
• Gold Metalization	• Aluminum Metalization
• Gold Beam Leads	• Al Wire Bonding in Flat-Pac
• MSI	• MSI
• No Commercial Equiv. (Pin Replaceable)	• Commercial Equiv.
• Vendors	• Vendors
- Motorola	- Harris
- RCA	- Fairchild (Terminated)
- TI	- TI

Figure 4.4

SAMPLE PARTS LIST

LMSC C-4

MSIA

1. 811* Quad 2 Input NAND
2. 812* Dual 4 Input NAND
3. 813* Dual JK Flip-Flop
4. 814* Op Amp
5. 815* Dual 4 to 1 MPXR
6. 816* Dual 2 to 4 Decoder
7. 817 4 x 4 Register File
8. 818† ALU
9. 819* 1024 Bit ROM
10. 820* Synchronous Up/Down Cntr.
11. 821* 4 Bit Bidirectional Shift Reg.
12. 822 64 x 1 RAM
13. 119 FET Driver

1. 4 Bit Bidirectional Shift Reg.
2. 2 Bit Binary Full Adder
3. Memory Driver
4. 3 to 8 Decoder
5. Dual 4 to 1 MPXR
6. 4 Bit Synchronous Counter

(*) - Required by AIRS

(†) - Mask change for XOR

Figure 4.5

The only transient upset tests performed to date on an LSI circuit are those of Boeing on the TI SB0400. An upset was observed at 2 to 3×10^7 rad (si)/sec. It is Questron's recommendation that similar tests be performed on the new 9900 I²L microprocessor to evaluate the effect of reduced device geometry.

Questron has suggested that NWSC include an LSI *logic* device in their technology assessment effort along with a RAM. Questron is currently holding discussions with integrated circuit houses regarding the fabrication of the GPU device recently designed and developed at RCA. This device is the highest performance bit slice available and, since it has both an ALU and register file on chip, it will make an excellent test bed for comparing various proposed LSI technologies.

At the International Reliability Conference in April, 1976, Bell Laboratories presented the point of view that I²L is essentially a common bipolar technology and as such, can easily be designed to whatever reliability levels achievable with T²L, LP Schottky, etc. A novel feature of I²L is that it can be operated below 1 volt V_{DD} (although it will be fairly slow) and that chemical electro-migration in a salt solution appears to have a 1 volt threshold. Thus, if the device is operated at less than 1 volt, neither chip passivation nor hermetic package seals would be required. Unfortunately, most I²L devices produced to date have T²L buffer circuits which operate at ~ 5 volts V_{DD} .

4.3 Memory Implementation

Program memory storage for guidance systems with hardening requirements has traditionally been a problem. Historically these subsystems have been cumbersome, unwieldy, and inefficient, due primarily to what was available as a developed hardened storage media. The Minuteman III employs a drum memory which is a serial memory and therefore far too slow for the ambitious requirements proposed for the next generation guidance machines. The Poseidon computer incorporates a U-Core "Braid" program memory which is very bulky and is a memory that requires a total new manufactured item when program changes are necessary.

The SP-23 Branch of the Navy has decided to use the integrated circuit Programmable Read-Only Memories (PROM) as the program memory for the Trident guidance computer. These devices will be commercial devices such as the Harris H7610 with the exception of NiCr film current limiting resistors on the chip and a gold doping for improved Beta performance under radiation. The memory system will employ power strobing after transient radiation to recover from any "latch-up" problems. It should be emphasized that Trident will take existing commercial PROMS on bulk silicon (no dielectric isolation) and add NiCr resistors and a gold spiking step for their devices. In the past, considerable concern has been given to the reliability aspects of PROM'S. The biggest fear has been the so called "regrowth" phenomenon of the links. CSDL's studies into this problem have revealed that the problem lies in the commercial economics of the device. When the NiCr links are put on the wafer there is often a mask registration problem and the routine procedure has been to strip off the NiCr, realign the mask, and redeposit the links. In stripping off the NiCr, the oxide on which it was deposited becomes etched into a stepped structure. Therefore when the NiCr is redeposited properly, the oxide steps create ultra thin links at each step. This weak point is what breaks during the programming of the PROM and since the opening is only a few angstroms wide, the so called "regrowth" is attributed to many factors. The point is that to prevent PROM regrowth, devices must be procured that have not had the NiCr stripped during the wafer processing.

The impact of the Navy program is significant to ABRES computer design activities. The use of commercial PROM'S, with small modifications, would result in a flexible semiconductor memory better serving the size, weight, and power aspects of reentry systems.